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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Exploiting skewed state probabilities for low power state assignment**
Bhupathi, I.; Chao, L.-F.;
Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium on , Volume: 4 , 12-15 May 1996
Pages:759 - 762 vol.4

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

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2 **Minimization of task turnaround time for distributed systems**
Chiun-Chieh Hsu; Sheng-De Wang; Te-Son Kuo;
Computer Software and Applications Conference, 1989. COMPSAC 89., Proceedi of the 13th Annual International , 20-22 Sept. 1989
Pages:2 - 7

[Abstract] [PDF Full-Text (356 KB)] **IEEE CNF**

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3 **Synthesis and optimization of asynchronous controllers based on extended lock graph theory**
Ykman-Couvreur, C.; Lin, B.; Goossens, G.; De Man, H.;
Design Automation, 1993, with the European Event in ASIC Design. Proceeding: [4th] European Conference on , 22-25 Feb. 1993
Pages:512 - 517

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9
Best 200 shown

1 Almost-optimum speed-ups of algorithms for bipartite matching and related
Harold Gabow, Robert Tarjan
January 1988 Proceedings of the twentieth annual ACM symposium on Theory o
Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, ci

We present algorithms for matching and related problems that run on an EREW bipartite graph G with n vertices, m edges, and integral edge costs at most N in assignment problem (minimum cost perfect bipartite matching) that runs in &Oc

2 Area optimization of multi-functional processing units
A. van der Werf, M. J. H. Peek, E. H. L. Aarts, J. L. van Meerbergen, P. E. R. Lippe
November 1992 Proceedings of the 1992 IEEE/ACM international conference on Com
Full text available: pdf(997.96 KB) Additional Information: full citation, references, citings, index

3 Assignment of global memory elements for multi-process VHDL specificatic
H. Krämer, J. Müller
November 1992 Proceedings of the 1992 IEEE/ACM international conference on Com
Full text available: pdf(685.87 KB) Additional Information: full citation, references, citings, index te

4 Efficient circuit partitioning algorithms for parallel logic simulation
S. Patil, P. Banerjee, C. Polychronopoulos
August 1989 Proceedings of the 1989 ACM/IEEE conference on Supercomputi
Full text available: pdf(959.59 KB) Additional Information: full citation, abstract, references,

General purpose parallel processing machines are increasingly being used to spe This paper addresses logic simulation on parallel machines by exploiting the con (called data parallelism) as opposed to exploiting parallelism inherent in the sim parallelism). The most crucial step in obtaining the maximum parallelism using

5 Platforms: DFuse: a framework for distributed data fusion
Rajnish Kumar, Matthew Wolenetz, Bikash Agarwalla, JunSuk Shin, Phillip Hutto, A
November 2003 Proceedings of the first international conference on Embedded ne
Full text available: pdf(541.24 KB) Additional Information: full citation, abstract, referen

Simple in-network data aggregation (or fusion) techniques for sensor networks research efforts, but they are insufficient to support advanced fusion application sensor networks and ask two related questions: (a) what is the appropriate set we dynamically assign aggregation roles to the nodes of a sensor network. We framework, *DFuse*, for ans ...

Keywords: data fusion, energy awareness, in-network aggregation, middleware, network

6 POSE: power optimization and synthesis environment
Sasan Iman, Massoud Pedram
June 1996 Proceedings of the 33rd annual conference on Design automation confer
Full text available: pdf(76.01 KB) Additional Information: full citation, references, citings, index terms

7 Automated phase assignment for the synthesis of low power domino circuit
Priyadarshan Patra, Unni Narayanan
June 1999 Proceedings of the 36th ACM/IEEE conference on Design automation con
Full text available: pdf(169.04 KB) Additional Information: full citation, references, citings, index terms

8 Register allocation for irregular architectures
Bernhard Scholz, Erik Eckstein
June 2002 ACM SIGPLAN Notices , Proceedings of the joint conference on Language systems: software and compilers for embedded systems, Volume 37 Iss
Full text available: pdf(220.34 KB) Additional Information: full citation, abstract, references,

For irregular architectures global register allocation is still a challenging problem far. The graph-coloring analogy of traditional approaches does not match the ne architectures which feature non-orthogonal instruction sets and small register fil new approach to global register allocation for irregular architectures. Our appro *partitioned boo ...*

Keywords: boolean quadratic problem, register allocation

9 Mini-buckets: A general scheme for bounded inference
Rina Dechter, Irina Rish
March 2003 Journal of the ACM (JACM), Volume 50 Issue 2
Full text available: pdf(902.27 KB) Additional Information: full citation, abstract, references,

This article presents a class of approximation algorithms that extend the idea of by successful constraint propagation algorithms, to probabilistic inference and c bound the dimensionality of dependencies created by inference algorithms. This *mini-buckets*, that offers adjustable trade-off between accuracy and efficiency. T problems, s ...

Keywords: Accuracy/complexity trade-off, Bayesian networks, approximation al probabilistic inference.

10 Optimal capacity and flow assignment for self-healing ATM networks basec
Kazutaka Murakami, Hyong S. Kim
April 1998 IEEE/ACM Transactions on Networking (TON), Volume 6 Issue 2
Full text available: pdf(435.33 KB) Additional Information: full citation, references, citing

Keywords: jointly optimal capacity and flow control, self healing networks, survi

11 Analysis techniques: A probabilistic analysis for the range assignment prob
Paolo Santi, Douglas M. Blough, Feodor Vainstein
October 2001 Proceedings of the 2nd ACM international symposium on Mobile ad h
Full text available: pdf(200.83 KB) Additional Information: full citation, abstract, references,

In this paper we consider the following problem for ad hoc networks: assume th *d*-dimensional region, with 1≤*d*≤3, and assume that all the nodes have the must *r* be to ensure that the resulting network is strongly connected? We study approach, and we establish lower and upper bounds on the probability of connec th ...

12 Optimal Dual -VT Assignment for Low-Voltage Energy-Constrained CMOS
Debasis Samanta, Ajit Pal
January 2002 Proceedings of the 2002 conference on Asia South Pacific design au
Full text available: pdf(288.23 KB) Publisher Site Additional Inform

In this paper we have addressed the problem of realizing dual-VT CMOS circuits portable systems. As the battery life is of primary concern, an algorithm is propo energy requirement in the standby mode as well as in the active mode, at the e algorithm for dual-VT assignment has been developed, which assigns high-VT tc the existing approaches, ...

13 Approximation algorithms for data placement in arbitrary networks
Ivan D. Baev, Rajmohan Rajaraman
January 2001 Proceedings of the twelfth annual ACM-SIAM symposium on Discre
Full text available: pdf(938.56 KB) Additional Information: full citation, abstract, references,

We study approximation algorithms for placing replicated data ir network of nodes with individual storage capacities and a metric which each node periodically issues a request for an object draw uniform-length objects. We consider the problem of placing copi nodes such that the average access cost is minimized. Our main constant-factor approximation algor ...

14 Technical correspondence: Efficient global register allocation for minimizing
Yumin Zhang, Xiaobo (Sharon) Hu, Danny Z. Chen
April 2002 ACM SIGPLAN Notices, Volume 37 Issue 4
Full text available: pdf(1.15 MB) Additional Information: full citation, abstract, re

Data referencing during program execution can be a significant source of energy data-intensive programs. In this paper, we propose an approach to minimize su to proper registers and memory. Through careful analysis of boundary condition approach efficiently handles various control structures including branches, merg results benefiting the whole program. The ...

Keywords: low energy, register allocation

15 Topology aggregation for directed graphs
Baruch Awerbuch, Yuval Shavitt
February 2001 IEEE/ACM Transactions on Networking (TON), Volume 9 Issue
Full text available: pdf(251.46 KB) Additional Information: full citation, references, citing

Keywords: PNNI, asynchronous transfer mode, communication system routing, wide-area networks

16 A code-motion pruning technique for global scheduling
Luiz C. V. Dos Santos, M. J. M. Heijligers, C. A. J. Van Eijk, J. Van Eijnhoven, J. A.
January 2000 ACM Transactions on Design Automation of Electronic Systems (TOD
Full text available: pdf(293.27 KB) Additional Information: full citation, abstract, references,

In the high-level synthesis of ASICs or in the code generation for ASIPs, the pre description represents an obstacle to exploit parallelism. Most existing methods search space is limited by the applied heuristics. For example, they might miss block boundaries when treating conditional execution. We propose a constructiv motions. Schedu ...

Keywords: code generation, code motion, global scheduling, high-level synthesis

17 Quality of service provision in noncooperative networks: heterogenous pref vectors, and burstiness
Kihong Park, Meera Sitharam, Shaogang Chen
October 1998 Proceedings of the first international conference on Information and
Full text available: pdf(1.98 MB) Additional Information: full citation, references, inde

18 Implicit computation of minimum-cost feedback-vertex sets for partial scan
Pranav Ashar, Sharad Malik
June 1994 Proceedings of the 31st annual conference on Design automation conf
Full text available: pdf(72.87 KB) Additional Information: full citation, references, citings, index

19 Register allocation and binding for low power
Jui-Ming Chang, Massoud Pedram
January 1995 Proceedings of the 32nd ACM/IEEE conference on Design automation c
Full text available: pdf(238.80 KB) Additional Information: full citation, references, citings, index terms

20 LP based approach to optimal stable matchings
Chung-Piaw Teo, Jay Sethuraman
January 1997 Proceedings of the eighth annual ACM-SIAM symposium on Discrete al
Full text available: pdf(1.06 MB) Additional Information: full citation, references, index terms

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7

Results 21 - 40 of 200 Result page: previous 1 **2** 3 4 5 6 7
Best 200 shown

21 Parallel compiled event driven VHDL simulation
V. Krishnaswamy, P. Banerjee
July 1998 Proceedings of the 12th international conference on Supercomputing
Full text available: pdf(964.02 KB) Additional Information: full citation, references, index terms

22 A Constructive Method for Exploiting Code Motion
Luiz C. V. dos Santos, M. J. M. Heijligers, C. A. J. Van Eijk, J. T. J. Van Eijndhoven,
November 1996 Proceedings of the 9th International Symposium on System S
Full text available: pdf(980.25 KB) Publisher Site Additional Inform

In this paper we address a resource-constrained optimization problem for behav
In high-level synthesis of ASICs or in code generation for ASIPs, most methods
search space is limited by the applied heuristics. For example, they might miss
block boundaries when treating conditional execution. We propose an approach
constructive method to al ...

Keywords: Code motion, conditionals, scheduling, high-level synthesis, code ger
search space pruning

23 Directed network design with orientation constraints
Sanjeev Khanna, Joseph Naor, F. Bruce Shepherd
February 2000 Proceedings of the eleventh annual ACM-SIAM symposium on Discrete
Full text available: pdf(871.10 KB) Additional Information: full citation, references, index terms

24 Automatic data layout for distributed-memory machines
Ken Kennedy, Ulrich Kremer
July 1998 ACM Transactions on Programming Languages and Systems (TOPLAS),
Full text available: pdf(633.20 KB) Additional Information: full citation, abstract, references, citi

The goal of languages like Fortran D or High Performance Fortran (HPF) is to pr machine-independent parallel programming model. After the algorithm selection intellectual challenge in writing an efficient program in such languages. The perf target compilation system, the target machine, the problem size, and the numb choice of a good layout extremel ...

Keywords: high performance Fortran

25 IMPACT: a high-level synthesis system for low power control-flow intensive
K. S. Khouri, G. Lakshminarayana, N. K. Jha
February 1998 Proceedings of the conference on Design, automation and test i
Full text available: pdf(186.38 KB) Publisher Site Additional Information: full citation, abstra

In this paper, we present a comprehensive high-level synthesis system that is g consumption in control-flow intensive circuits. An iterative improvement algorith algorithm searches the design space by handling scheduling, module selection, r restructuring simultaneously. The scheduler performs concurrent loop optimizati minimizes the expected number of cycles o ...

Keywords: low power, control-flow, high-level synthesis, multiplexer re-structur

26 A software engineering perspective on algorithmics
Karsten Weihe
March 2001 ACM Computing Surveys (CSUR), Volume 33 Issue 1
Full text available: pdf(1.62 MB) Additional Information: full citation, abstract, references, in

An algorithm component is an implementation of an algorithm which is not inter perform a specific task within a large software package or even within several d design of algorithm components must also incorporate software-engineering asp This goal is important for maintenance throughout a project, prototypical develo contex ...

Keywords: algorithm engineering

27 Models of machines and computation for mapping in multicomputers
Michael G. Norman, Peter Thanisch
September 1993 ACM Computing Surveys (CSUR), Volume 25 Issue 3
Full text available: pdf(3.49 MB) Additional Information: full citation, references, citings, index terms

Keywords: mapping, multicomputer load balancing, multicomputers, partitioning

28 PathFinder: a negotiation-based performance-driven router for FPGAs
Larry McMurchie, Carl Ebeling
February 1995 Proceedings of the 1995 ACM third international symposium on Field
Full text available: pdf(76.11 KB) Additional Information: full citation, abstract, references, c

Routing FPGAs is a challenging problem because of the relative scarcity of routir points. This can lead either to slow implementations caused by long wiring paths route all signals. This paper presents PathFinder, a router that balances the goa PathFinder uses an iterative algorithm that converges to a solution in which all s the optimal per ...

29 Stackelberg scheduling strategies
Tim Roughgarden
July 2001 Proceedings of the thirty-third annual ACM symposium on Theory of c
Full text available: pdf(230.68 KB) Additional Information: full citation, abstract, references,

We study the problem of optimizing the performance of a system shared by self the concrete setting of scheduling jobs on a set of shared machines with load-de length of time necessary to complete a job; we measure system performance by jobs according to the selfish interests of individual users (who wish to minimize

30 Virtual path routing for survivable ATM networks
Kazutaka Murakami, Hyong S. Kim
February 1996 IEEE/ACM Transactions on Networking (TON), Volume 4 Issue 1
Full text available: pdf(2.24 MB) Additional Information: full citation, references, citings, index terms

31 Divide-and-conquer approximation algorithms via spreading metrics
Guy Even, Joseph Seffi Naor, Satish Rao, Baruch Schieber
July 2000 Journal of the ACM (JACM), Volume 47 Issue 4
Full text available: pdf(320.60 KB) Additional Information: full citation, abstract, references, citi

We present a novel divide-and-conquer paradigm for approximating NP-hard gr models graph optimization problems that satisfy two properties: First, a divide-a Second, a fractional spreading metric is computable in polynomial time. The spr edges or vertices of the input graph, such that all subgraphs for which the optir diameters. In addition, ...

Keywords: approximation algorithms, divide and conquer, feedback set, linear a

32 An iterative improvement algorithm for low power data path synthesis
Anand Raghunathan, Niraj K. Jha
December 1995 Proceedings of the 1995 IEEE/ACM international conference on C
Full text available: pdf(172.45 KB) Publisher Site Additional Information: full citation, abstra

We address the problem of minimizing power consumption in behavioral synthes complex nature of power as a cost function implies that the effects of several be selection, clock selection, scheduling, and resource sharing on supply voltage ar considered simultaneously to fully derive the benefits of design space exploratio established the importance of beha ...

Keywords: Behavioral synthesis, Low power VLSI design, Power consumption

33 Lower and upper bounds on the switching activity in scheduled data flow gr
Lars Kruse, Eike Schmidt, Gerd Jochens, Wolfgang Nebel
August 1999 Proceedings of the 1999 international symposium on Low power electr
Full text available: pdf(702.48 KB) Additional Information: full citation, references, citings, index ter

Keywords: bounds estimation, high-level power estimation

34 Chip-level area routing

Le-Chin Eugene Liu, Hsiao-Ping Tseng, Carl Sechen

April 1998 Proceedings of the 1998 international symposium on Physical desigr

Full text available: pdf(1.24 MB) Additional Information: full citation, abstract, references, cit

We present a chip-level area router for modern VLSI technologies. The gridless layers, as well as rectilinear blockage areas on any layer. A two-stage divide-an area router can handle very large chips. The first stage includes an area-minimi: accurate multi-layer global router. The global router minimizes the chip area wh According to the global ...

35 Combining fairness with throughput: online routing with multiple objectives

Ashish Goel, Adam Meyerson, Serge Plotkin

May 1999 Proceedings of the thirty-second annual ACM symposium on Theory of co

Full text available: pdf(1.05 MB) Additional Information: full citation, references, citings, index terms

36 Routing II: Throughput-centric routing algorithm design

Brian Towles, William J. Dally, Stephen Boyd

June 2003 Proceedings of the fifteenth annual ACM symposium on Parallel algorith

Full text available: pdf(153.68 KB) Additional Information: full citation, abstract, referenc

The increasing application space of interconnection networks now encompasses routing and I/O interconnect, where the throughput of a routing algorithm, not j performance metric. We show that the problem of designing oblivious routing al average-case throughput can be cast as a linear program. Globally optimal solut be efficiently found, yielding p ...

Keywords: interconnection networks, multicommodity flows, oblivious routing

37 Optimizing exact genetic linkage computations

Maáyan Fishelson, Dan Geiger

April 2003 Proceedings of the seventh annual international conference on Computa

Full text available: pdf(188.29 KB) Additional Information: full citation, abstract, referen

Genetic linkage analysis is a challenging application which requires Bayesian net Consequently, computing the likelihood of data, which is needed for learning linl procedures calls for an extremely efficient implementation that carefully optimiz summation operations. In this paper we present the use of stochastic greedy alg algorithm has been incorp ...

Keywords: DAG models, bayesian networks, combinatorial optimization, genetic probabilistic algorithms, superlink, treewidth

38 Simultaneous reference allocation in code generation for dual data memory
Ashok Sudarsanam, Sharad Malik
April 2000 ACM Transactions on Design Automation of Electronic Systems (TODAE
Full text available: pdf(156.30 KB) Additional Information: full citation, abstract, references,

We address the problem of code generation for DSP systems on a chip. In such program ROM is limited, so application software must be sufficiently dense. Add as to meet various high-performance constraints, which may include hard real-t compiler technology is unable to generate high-quality code for DSPs, whose arc designers often r ...

Keywords: code generation, code optimization, graph labelling, memory bank as

39 Fusion-based register allocation
Guei-Yuan Lueh, Thomas Gross, Ali-Reza Adl-Tabatabai
May 2000 ACM Transactions on Programming Languages and Systems (TOPLAS),
Full text available: pdf(475.45 KB) Additional Information: full citation, abstract, references, citi

The register allocation phase of a compiler maps live ranges of a program to rec there are physical registers, the register allocator must spill a live range (the ho range (the live range occupies multiple locations). One of the challenges for a re splitting together. Fusion-based register allocation uses the structure of the proc

Keywords: performance evaluation, register allocation

40 A novel approach towards automatic data distribution
Jordi Garcia, Eduard Ayguadé, Jesus Lebarta
December 1995 Proceedings of the 1995 ACM/IEEE conference on Supercomputing (
Full text available: pdf(172.14 KB) html(2.44 KB) Additional Information: full citation, references, citings, ir

Results 41 - 60 of 200 Result page: previous 1 2 **3** 4 5 6 7
Best 200 shown

41 An efficient algorithm for image segmentation, Markov random fields and re
Dorit S. Hochbaum
July 2001 Journal of the ACM (JACM), Volume 48 Issue 4
Full text available: pdf(174.92 KB) Additional Information: full citation, abstract, references,

Problems of statistical inference involve the adjustment of sample observations requirements, or order constraints. In such problems, the objective is to minimi: depends on the distance between the observed value and the modify value. In M also a pairwise relationship between the objects. The objective in Markov randoı the deviation cost function an ...

Keywords: Convex optimization, Markov random fields, parametric minimum cut

42 Implementing the MPI process topology mechanism
Jesper Larsson Träff
November 2002 Proceedings of the 2002 ACM/IEEE conference on Supercomp
Full text available: pdf(165.65 KB) Additional Information: full citation, abstract, referenc

The topology functionality of the *Message Passing Interface* (MPI) provides a po for adapting application programs to the communication architecture of the targ implementations rarely go beyond the most trivial implementation, and simply p discuss the potential of the topology mechanism for systems with a hierarchical of SMP nodes. The MPI topology ...

43 High-level power estimation (invited talks): Lower bound estimation for low
Lars Kruse, Eike Schmidt, Gerd Jochens, Ansgar Stammermann, Wolfgang Nebel
September 2000 Proceedings of the 13th international symposium on System s
Full text available: pdf(53.04 KB) Additional Information: full citation, abstract, referer

This paper addresses the problem of estimating lower bounds on the power con: with a fixed number of allocated resources prior to binding. The estimated boun resource sharing. It is shown that by introducing Lagrangian multipliers and rela the Assignment Problem, which can be solved in $O(n^3)$, a tight and fast computa results show the good qu ...

44 Drawing graphs nicely using simulated annealing
Ron Davidson, David Harel
October 1996 ACM Transactions on Graphics (TOG), Volume 15 Issue 4
Full text available: pdf(456.49 KB) Additional Information: full citation, abstract, references,

The paradigm of simulated annealing is applied to the problem of drawing graph deals with general undirected graphs with straight-line edges, and employs seve of the result. The algorithm is flexible, in that the relative weights of the criteria size it produces good results, competitive with those produced by other method: method” and its ...

Keywords: aesthetics, graph drawing, simulated annealing

45 Emerald: an architecture-driven tool compiler for FPGAs
Darren C. Cronquist, Larry McMurchie
February 1996 Proceedings of the 1996 ACM fourth international symposium on Field
Full text available: pdf(212.36 KB) Additional Information: full citation, references, citings, inc

46 Concurrency preserving partitioning (CPP) for parallel logic simulation
Hong K. Kim, Jack Jean
July 1996 ACM SIGSIM Simulation Digest , Proceedings of the tenth workshop on Pa 26 Issue 1
Full text available: pdf(855.09 KB) Publisher Site Additional Information: full citation, abstr

Based on a linear ordering of vertices in a directed graph, a linear-time partition is presented. Unlike most other partitioning algorithms, the proposed algorithm to processors circuit gates that can be evaluated at about the same time. As a r partitioning (CPP) algorithm can provide better load balancing throughout the pe especially import ...

Keywords: Parallel Logic Simulation, Partitioning, Concurrency, Load Balancing,

47 Reduction of compilation costs through language contraction
Mary Shaw
May 1974 Communications of the ACM, Volume 17 Issue 5
Full text available: pdf(502.07 KB) Additional Information: full citation, abstract, referenc

Programming languages tailored to particular groups of users can often be consi from a general purpose language. This paper describes the use of simulation tec compilation cost achievable by such an approach. The results suggest a function the power of a language on the compilation cost of an algorithm expressed in th used by the algorithm are ...

Keywords: Algol, compilation cost, compiler design, design of programming lanc

48 Virtual path control for ATM networks with call level quality of service guara
Nikolaos Anerousis, Aurel A. Lazar
April 1998 IEEE/ACM Transactions on Networking (TON), Volume 6 Issue 2
Full text available: pdf(446.53 KB) Additional Information: full citation, references, citings, index terms

49 A new viewpoint on code generation for directed acyclic graphs
S. Liao, K. Keutzer, S. Tjiang, S. Devadas
January 1998 ACM Transactions on Design Automation of Electronic Systems (TOD
Full text available: pdf(661.59 KB) Additional Information: full citation, abstract, referenc

We present a new viewpoint on code generation for directed acyclic graphs (DA(covering, the problem of satisfying, with minimum cost, a set of disjunctive clau commutativity of operators and of the machine model. An important contributio sufficient conditions for a valid schedule to be derived, based on the notion of w

Keywords: binate covering, code generation, directed acyclic graphs

50 Behavioral synthesis of field programmable analog array circuits
Haibo Wang, Sarma B. K. Vrudhula
October 2002 ACM Transactions on Design Automation of Electronic Systems (TOD
Full text available: pdf(519.64 KB) Additional Information: full citation, abstract, referen

This article presents methods to translate a behavioral-level analog description i (FPAA) implementation. The methods consist of several steps that are referred t synthesis, placement and routing, and postplacement simulation. The focus of tl function decomposition step deals with decomposing a high-order system functi present an efficien ...

Keywords: Programmable circuits, analog synthesis

51 Faster scaling algorithms for general graph matching problems
Harold N. Gablow, Robert E. Tarjan
October 1991 Journal of the ACM (JACM), Volume 38 Issue 4
Full text available: pdf(2.87 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: augmenting path, blossoms matching, network optimisation, scaling

52 Optimal design of survivable mesh networks based on line switched WDM
Andrea Fumagalli, Isabella Cerutti, Marco Tacca
June 2003 IEEE/ACM Transactions on Networking (TON), Volume 11 Issue 3
Full text available: pdf(522.20 KB) Additional Information: full citation, abstract, referen

Network survivability provided at the optical layer is a desirable feature in mode wavelength division multiplexed (WDM) self-healing ring (or SHR/WDM) provide protection mechanism against any single fault in the ring. Multiple self-healing ri survivable optical mesh network by superposing a set of rings on the arbitrary t such a network requires ...

Keywords: self-healing ring, shared-line protection, survivability, wavelength co

53 VLSI leaf cell design by understanding circuit structures
W. Lue, L. D. McNamee
June 1989 Proceedings of the second international conference on Industrial and eng intelligence and expert systems - Volume 1
Full text available: pdf(988.12 KB) Additional Information: full citation, abstract, referen

A new approach utilizing MOS circuit structures extracted from a circuit net-list f circuit structure is explicitly present in a circuit schematic diagram on which a d However, it is absent in the net-list input to an automatic layout system. In this information from a net-list and how to apply it for automatic leaf cell design are

54 Sequential Permissible Functions and their Application to Circuit Optimizati
Chih-chang Lin, Malgorzata Marek-Sadowska, Kuang-Chien Chen, Mike Tien-Chien
March 1996 Proceedings of the 1996 European conference on Design and Tes
Full text available: pdf(783.44 KB) Publisher Site Additional Inform

For sequential circuits the implementation freedom represented by combinationa un-reachable states don't cares is not complete. We extend the concept of perm introduce the sequential permissible functions (SPFs) to represent the complete study and compare the relationship between CPFs and SPFs. In general, the con than the computation of CPFs ...

Keywords: permissible functions, sequential permissible functions, logic optimiza

55 New parallelization and convergence results for NC: a negotiation-based FI
Pak K. Chan, Martine D. F. Schlag
February 2000 Proceedings of the 2000 ACM/SIGDA eighth international symposium
Full text available: pdf(953.15 KB) Additional Information: full citation, abstract, references,

The negotiation-based routing paradigm has been used successfully in a numbei several new findings related to the negotiation-based routing paradigm. We exa negotiation-based routing algorithm. We illustrate that the negotiation-based alg demonstrate that a negotiation-based parallel FPGA router can perform well in t FPGA circui ...

56 Efficient scheduling of conditional behaviors for high-level synthesis
Apostolos A. Kountouris, Christophe Wolinski
July 2002 ACM Transactions on Design Automation of Electronic Systems (TODAES
Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references

As hardware designs get increasingly complex and time-to-market constraints g high-level synthesis (HLS). HLS must efficiently handle both dataflow-dominatec well as designs of a mixed nature. In the past efficient tools for the former type conditional behaviors lags behind. To bridge this gap an efficient scheduling heu presented. Our heuristic a ...

Keywords: Design automation, conditional behavior, high level synthesis (HLS),

57 Data-flow assisted behavioral partitioning for embedded systems
Samir Agrawal, Rajesh K. Gupta
June 1997 Proceedings of the 34th annual conference on Design automation confere
Full text available: pdf(88.40 KB) Additional Information: full citation, references, citings, index terms

58 Session 7B: The price of anarchy is independent of the network topology
Tim Roughgarden
May 2002 Proceedings of the thiry-fourth annual ACM symposium on Theory of c
Full text available: pdf(245.18 KB) Additional Information: full citation, abstract, references,

We study the degradation in network performance caused by the selfish behavic consider a directed network in which each edge possesses a latency function de: all traffic on the edge as a function of the edge congestion. Given a rate of traffi network, we aspire toward an assignment of traffic to paths in which the sum of minimized; however, ...

59 Sequential synthesis for table look up programmable gate arrays
Rajeev Murgai, Robert K. Brayton, Albert Sangiovanni-Vincentelli
July 1993 Proceedings of the 30th international on Design automation conference
Full text available: pdf(786.69 KB) Additional Information: full citation, references, citings, index terms

60 Query evaluation techniques for large databases
Goetz Graefe
June 1993 ACM Computing Surveys (CSUR), Volume 25 Issue 2
Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citing

Database management systems will continue to manage large data volumes. Th manipulating large sets and sequences will be required to provide acceptable pe and extensible database systems will not solve this problem. On the contrary, m problem: In order to manipulate large sets of complex objects as efficiently as t simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, ex object-oriented database systems, operator model of parallelization, parallel alg set-matching algorithms, sort-hash duality

USPTO Patent Full-Text and Image Database

Searching 1790 to present...

Results of Search in 1790 to present db for:
(("directed graph" AND "assignment") AND "cost function"): 21 patents.
Hits 1 through 21 out of 21

Jump To

Refine Search "directed graph" and "assignment" and "cost functi

	PAT. NO.	Title
1	6,654,354	System and method for planning multiple MUX levels in a fiber optic network simulation plan
2	6,556,962	Method for reducing network costs and its application to domino circuits
3	6,545,977	Methods and apparatus for routing signals in a ring network
4	6,529,861	Power consumption reduction for domino circuits
5	6,480,991	Timing-driven global placement based on geometry-aware timing budgets
6	6,373,971	Method and apparatus for pattern discovery in protein sequences
7	6,308,299	Method and system for combinational verification having tight integration of verification techniques
8	6,226,627	Method and system for constructing adaptive and resilient software
9	6,108,666	Method and apparatus for pattern discovery in 1-dimensional event streams
10	6,092,065	Method and apparatus for discovery, clustering and classification of patterns in 1-dimensional event streams
11	6,088,689	Multiple-agent hybrid control architecture for intelligent real-time control of distributed nonlinear processes
12	5,977,890	Method and apparatus for data compression utilizing efficient pattern discovery
13	5,963,447	Multiple-agent hybrid control architecture for intelligent real-time control of distributed nonlinear processes
14	5,918,035	Method for processor modeling in code generation and instruction set simulation
15	5,742,814	Background memory allocation for multi-dimensional signal processing
16	5,671,403	Iterative dynamic programming system for query optimization with bounded complexity
17	5,659,796	System for randomly modifying virtual channel allocation and accepting the random modification based on the cost function

18 5,522,063 [I] Method of finding minimum-cost feedback-vertex sets for a graph for partial scan testing without exhaustive cycle enumeration

19 5,418,953 [T] Method for automated deployment of a software program onto a multi-processor architecture

20 5,021,947 [T] Data-flow multiprocessor architecture with three dimensional multistage interconnection network for efficient signal and data processing

21 5,005,136 [T] Silicon-compiler method and arrangement

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